



## CE-ATA Technical Errata

<b>Errata ID</b>	<b>Protocol 018</b>
<b>Affected Spec Ver.</b>	<b>Protocol 1.0</b>
<b>Corrected Spec Ver.</b>	

### Submission info

Name	Company	Date
Amber Huffman	Intel	10/14/2005

### Description of the specification technical flaw (add space as needed)

The appendix that shows ATA command examples has inaccurate values for bit 6 of the Device register. Bit 6 of the Device register is reserved for READ DMA EXT and WRITE DMA EXT commands in CE-ATA, since all commands only use LBA addressing. This erratum corrects the example in the appendix to follow the ATA command definitions.

[illegible]

**Figure 36 shall be modified as shown:**

Address	Register	7	6	5	4	3	2	1	0
0h	Reserved	0							
1h	Features (exp)	0							
2h	Sector Count (exp)	0							
3h	LBA Low (exp)	0							
4h	LBA Mid (exp)	0							
5h	LBA High (exp)	0							
6h	Control	0					0	0	0
7h	Reserved	0							
8h	Reserved	0							
9h	Features	0							
Ah	Sector Count	10h							
Bh	LBA Low	0							
Ch	LBA Mid	1h							
Dh	LBA High	0							
Eh	Device/Head	0	4 0	0	0	0			
Fh	Command	25h							

**Figure 40 shall be modified as shown:**

Address	Register	7	6	5	4	3	2	1	0
0h	Reserved	0							
1h	Features (exp)	0							
2h	Sector Count (exp)	0							
3h	LBA Low (exp)	0							
4h	LBA Mid (exp)	0							
5h	LBA High (exp)	0							
6h	Control	0					0	0	0
7h	Reserved	0							
8h	Reserved	0							
9h	Features	0							
Ah	Sector Count	8h							
Bh	LBA Low	0							
Ch	LBA Mid	1h							
Dh	LBA High	0							
Eh	Device/Head	0	4 0	0	0	0			
Fh	Command	35h							

#### Disposition log

10/14/2005	Erratum captured
1/12/2006	Erratum ratified

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